Claims

What is claimed is:

1. A voltage-controlled delay line, comprising:

a delay element; and

a phase interpolation circuit coupled to the delay element;

wherein the delay element and the phase interpolation circuit are operative to: (i) obtain an input signal and a complement of the input signal; and (ii) use the input signal and the complement of the input signal to perform a phase interpolation process so as to realize a complete delay tuning range with respect to the input signal.

2. The voltage-controlled delay line of claim 1, wherein the phase interpolation process is a second-order phase interpolation process.

3. The voltage-controlled delay line of claim 1, wherein the delay tuning range is equivalent to 180 degrees of a period of the input signal.

4. The voltage-controlled delay line of claim 1, wherein the delay tuning range is guaranteed over a process variation.

5. The voltage-controlled delay line of claim 1, wherein the delay tuning range is guaranteed over a temperature variation.

6. The voltage-controlled delay line of claim 1, wherein the complement of the input signal is used to generate an absolute 180-degree phase reference.

7. A a delay-locked loop circuit, comprising:

a voltage-controlled delay line comprising: (i) a delay element; and (ii) a phase interpolation circuit coupled to the delay element; wherein the delay element and the phase interpolation circuit are operative to obtain an input signal and a complement of the input signal; and use the input signal and the complement of the input signal to perform a phase interpolation process so as to realize a complete delay tuning range with respect to the input signal; and

a phase detector coupled to the voltage-controlled delay line for generating an error signal for adjusting a phase shift associated with the voltage-controlled delay line.

8. A clock and data recovery system, comprising:

a clock recovery circuit for recovering a clock signal;

a voltage-controlled delay line, coupled to the clock recovery circuit, comprising: (i) a delay element; and (ii) a phase interpolation circuit coupled to the delay element; wherein the delay element and the phase interpolation circuit are operative to obtain the clock signal and a complement of the clock signal; and use the clock signal and the complement of the clock signal to perform a phase interpolation process so as to realize a complete delay tuning range with respect to the clock signal; and

a data recovery circuit coupled to the voltage-controlled delay line for recovering data in accordance with a clock signal received from the voltage-controlled delay line.

9. A method for delaying an input signal, comprising the steps of:

obtaining an input signal and a complement of the input signal; and

using the input signal and the complement of the input signal to perform a phase interpolation process so as to realize a complete delay tuning range with respect to the input signal.

10. The method of claim 9, wherein the phase interpolation process is a second-order phase interpolation process.

11. The method of claim 9, wherein the delay tuning range is equivalent to 180 degrees of a period of the input signal.

12. The method of claim 9, wherein the delay tuning range is guaranteed over a process variation.

13. The method of claim 9, wherein the delay tuning range is guaranteed over a temperature variation.

14. The method of claim 9, wherein the complement of the input signal is used to generate an absolute 180-degree phase reference.

15. Apparatus for delaying an input signal, comprising:

a memory; and

at least one processor coupled to the memory and operative to: (i) obtain an input signal and a complement of the input signal; and (ii) use the input signal and the complement of the input signal to perform a phase interpolation process so as to realize a complete delay tuning range with respect to the input signal.